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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,660	07/22/2003	Hisao Koyanagi	Q76637	4753

23373 7590 09/14/2005

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,660	KOYANAGI, HISAO	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-16* is/are rejected.

7)☐ Claim(s) *6,7,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/22/03 6/2/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-18 are in the application.

Claims 1-5,8-16 are rejected.

Claims 6-7,17-18 are objected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,8-14 rejected under 35 U.S.C. 103(a) as being unpatentable over Omoda et al (US 4680730) in view of Suzuki (US 6240524), and further in view of Nishi (US 5241633).

As for claim 1, Omoda describes a vector information processing apparatus comprising: a CPU comprising a plurality of asynchronously operating units (Omoda's Fig 12: #4 Vector Unit); a main memory for storing data (Omoda's Fig 12: #1-4); and a main memory controller for controlling the writing of data in said main memory (Omoda's Fig 12: #7), said main memory controller having a VSC address buffer (Omoda's Fig 12: #21 request stack) for holding

a storage address in said main memory for each element designated by a vector scatter instruction (Omoda's column 3 lines 45-55; request information comprises data element read/write request signal, memory address, stored data and request order (read/write identification information). Omoda does not describe the claim's detail of asynchronous operating units. However Suzuki describes a processor with multiple functional units (Suzuki's Fig 11: #90, #92 ALU units; column 11 lines 22-33) operating asynchronously (Suzuki's column 11, lines 45-52). It would have been obvious to one of ordinary skill in the art at the time of invention to include asynchronously functional units as suggested by Suzuki in Omoda's system in order to shorten the clock period of these functional units, hence these functional units can execute with faster clocks thereby elevate performance of the processor (Suzuki's column 2 lines 30-40).

The claim further describes for inhibiting the outputting of a writing permission signal for said main memory which is generated according to a writing request for writing an element having a smaller element number, which has the same storage address and which has not been processed in a sequence of element numbers, of writing requests for writing elements in said main memory which are issued respectively from said asynchronously operating units according to a vector scatter instruction. The claim appears to describe a situation whereas the memory store requests from the asynchronously operating units arrive at the memory in an out of order manner. Therefore the memory unit must process the requests according to the order they were original requested. Omoda describes the request order information to be used to transfer requests sequentially to memory (Omoda's column 3, lines 45-55). Omoda does not describe the address contention aspect of the claim. However Nishi describes a circuit to detect the address contention

for requests to a memory (Nishi's column 10 line 65 to column 11 line 20). It would have been obvious to one of ordinary skill in the art at the time of invention to include address contention detection circuit as suggested by Nishi in Omoda's system in order for prevent out of order passing of memory store instructions which having address contention (Nishi's column 10 line 65 to column 11 line 4).

As for claim 2, the claim rejected based on the same rationale as in the rejection of claim 1. Omoda futher describes wherein said main memory controller has a plurality of VSC address buffers corresponding respectively to said asynchronously operating units (Omoda's column 3 lines 45-55; request information comprises data element read/write request signal, memory address, stored data and request order (read/write identification information).

As for claim 3, Omoda describes wherein said asynchronously operating units impart one identifier to a plurality of said writing requests issued according to a single vector scatter instruction, and said main memory controller clears the contents of said VSC address buffers if an identifier of a preceding writing request and an identifier of a following writing request do not agree with each other (Omoda's column 1 lines 17-42).

As for claims 8-10, the claims recite wherein the number of storage addresses held by said VSC address buffer is set to at least (the number of elements simultaneously processed by said asynchronously operating unit)+1. Although Omoda and Suzuki do not describe the claim's detail of the size of the memory's received requests buffer. It is obviously that buffer size should be more that the number of requests being issued parallel from operating units of a vector processor in order to prevent the buffer being overflowed by receiving these simultaneously requests.

Claim 11 rejected based on the same rationale as in the rejection of claim 1.

Claim 12 rejected based on the same rationale as in the rejection of claim 2.

Claims 13-14 rejected based on the same rationale as in the rejection of claim 3.

Claims 4-5,15-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Omoda et al (US 4680730), Suzuki (US 6240524), Nishi (US 5241633) as applied to claims 3 and 11 respectively, and further in view of Lee at el (US 6629271).

As for claims 4-5 the claims recites wherein said main memory controller comprises: a VSC address buffer controller for controlling said VSC address buffer to hold said storage address sent from said asynchronously operating units and, if said VSC address buffer suffers an overflow, requests the asynchronously operating unit which has issued a vector scatter instruction that has caused said overflow to resend said element; and wherein said asynchronously operating unit has a retry buffer for holding each element designated by said vector scatter instruction issued thereby, and resends an element held by said retry buffer to said main memory controller if requested by said main memory controller to resend said element (claim 4); wherein said asynchronously operating unit corrects the element number of an element which starts to be resent based on a smallest element number, of the elements which start to be resent by each asynchronously operating unit (claim 5). Omoda does not describe the claim's detail of a retry buffer. However, Lee describes a processor with a replay system capable of keeping track of instructions being issued by the processor. Replay system detects the instructions that are not being executed properly and reissues them for re-execution (Lee's column 6, lines 27-45). It would have been obvious to one of ordinary skill in the art at the time

of invention to include a replay system as suggested by Lee in Omoda's system in order to re-executing the instructions in a proper order manner (Lee's column 6 lines 41-45).

Claims 15-16 rejected based on the same rationale as in the rejection of claims 4-5 correspondingly.

Allowable Subject Matter

Claims 6-7,17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claim 6 recites "wherein if said main memory controller detects a deadlock state in which an overflow of said VSC address buffer and a resending of an element from said asynchronously operating unit are repeated, said main memory controller sends a delay value for shifting the timing to resend the element from said asynchronously operating unit to said asynchronously operating unit; and wherein said asynchronously operating unit delays the timing to resend the element by said delay value received from said main memory controller".

The combination of above features is not found in the prior art of record.

Claims 7,17-18 have similar limitations as in claim 6.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Koyanagi (US Pub 2002/0007449) describes vector scatter and address contention detecting circuit.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin L. Ellis
Primary Examiner